Estimation of detrimental impact of new metals candidate in advanced microelectronic

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Introduction

The increasing complexity and miniaturization of integrated circuits (IC) requires the introduction of a large number of new materials which represent possible risk of contamination. Indeed many integration steps use "exotic metals" to achieve the targeted device performance:

- The transistor includes high-k dielectrics to replace SiO_2, silicides to replace the polycrystalline Si gate, metals for electrodes, substrates with high mobility.
- Interconnects need new barriers for Copper.
- Non-volatile memories and Above IC components such as RF features or imagers introduce new materials to target specific electrical, magnetic or optical properties.

Thus, considering also the "conventional" contaminants related to equipments, fluids and human activity, the periodic table of element in figure 1 gives an overview of metal specifies that will be used in advanced microelectronics and applications in which they could appear.

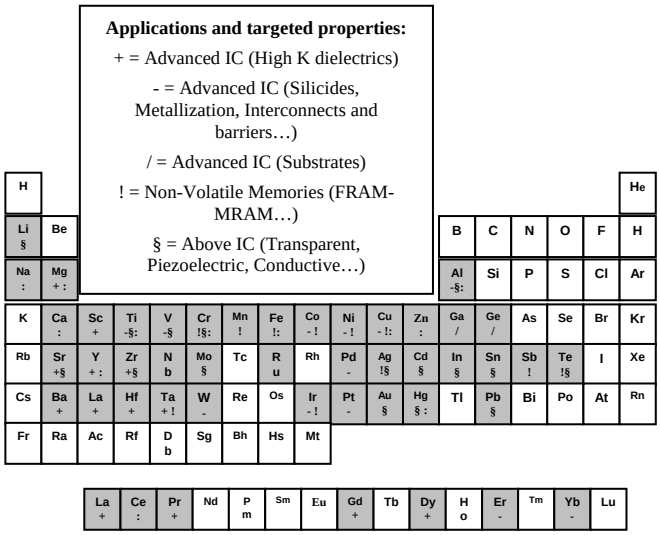

Figure1: List of candidates under investigation for integration in advanced microelectronics

This study follows work published in 2005 by Bigot et al. [1] and will focus on the behavior of each element toward Si and SiO_2 properties. This work aims at completing previous work dealing with the seriousness of cross contamination and will report for the first time with "news" metals for which the behavior in Silicon and oxide is really unknown (Sc, Er, Yb, La, Cd,…).

Impact of contaminants on devices

Despite contamination by Fe, Cu, Ca, Cr, Ni, Mo, Au… has been widely studied [2], possible damages on devices induced by "exotic" contaminants still need to be investigated. From fig.1, we can conclude that the full understanding of detrimental impact of every contaminant on each technology is almost impossible. Accordingly we put the emphasis on the impact of metals on Si and SiO_2 properties using physical short loops.

Experimental details (physical short loops)

Cz, 200 mm, (100) silicon wafers were intentionally contaminated with one metal (see list Fig.1). Three levels of contamination are targeted: 10^{11}, 10^{12} and 10^{13} at/cm². Wafers were cleaned using modified RCA leading to a contamination-free SiO_2 surface. Elements were deposited on the clean chemical oxide using the spin-drying technique. Then, wafers are oxidized at 950°C to obtain a 20 nm thick oxide and to drive in metals. The thermal oxidation is followed by an hydrogen annealing in order to saturate the dangling bonds of the surface and make a good interface passivation.

The impact of contaminants on Si and SiO_2 properties was evaluated by surface, interface and bulk analysis:

- Silicon lifetime measurements by microwave Photo-Conductivity Decay (µPCD, bulk and interface contribution),
- Accurate SiO_2 thickness measurements by spectroscopic ellipsometry (SE),
- Surface contamination analysis by Total-reflection X-Ray Fluorescence (TXRF) and global SiO_2 contamination by Vapor Phase Decomposition – Inductively Coupled Mass Spectrometry (VPD – ICPMS). Comparison on both techniques allows us to

estimate the ratio of contamination which had diffused in the silicon during the thermal treatment,

- Roughness analysis by Atomic Force Microscopy (AFM) and light scattering (Haze),
- Oxide integrity by C(V) and I(V) tests using a Mercury probe.

Results & Discussion

This study follows the idea of metal classification depending on behavior toward Si/SiO_2. Fig.2 and table.1 give an example of result. The references [1,2] propose a metal classification in 3 categories: the ones with a low diffusivity or solubility which stay inside the oxide or at the interface (group 1: Ca, Na, Hf, Ge, Zr, Y, La, Er…), the ones which diffuse in the silicon, have a high solubility and /or precipitate during the cooling (group 2 : Ti, Cr, Mn, Co, Cu, W…), and those which diffuse in the silicon and remain dissolved (group 3: Fe, Mo, Ru, Ir…).

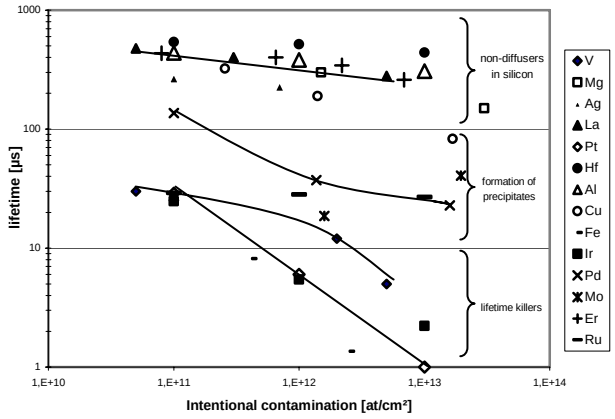

Figure 2: Influence of contaminants on µPCD-lifetime

The lifetime measurements permit to distinguish the three categories (see fig.1). Concerning the first group we can expect that during integration steps, they stay at the surface of the silicon and have detrimental impact mainly on SiO_2 and Si/SiO_2 interface. This is illustrated in Fig. 1 with lifetime measurements: values for wafers contaminated up to a few 10^{13} at/cm^2 are almost equal to the reference level (300+/-100µs). Metals from the second group can be fast diffuser (Cu, Ni, Co: 10^{-4} to 10^{-5} cm^2/s; Cr, Mn about 10^{-6} cm^2/s at 950°C) or slow diffuser (Ta, W, Ti, Sn: < 10^{-10} cm^2/s at 950°C). The first ones create precipitates with Si during cooling, making Si – rich ($NiSi_2$) or metal – rich silicides (Cu_3Si), while the second ones form oxide precipitates Thus, both types of metals from group 2 degrade µPCD lifetime, being damageable on the bulk and/or the interface. Metals from the third group are known to remain dissolved in Si in interstitial or substitutional sites. Thus, they are serious lifetime killers even after contamination below 10^{11} at/cm^2.

A proof of contamination being in SiO_2 only is brought by VPD-ICPMS analysis performed after oxidation compared to TXRF measurements performed after the contamination step (see table1). The reliability of measurements and results is assured by the matching of both techniques (+/- 5%).

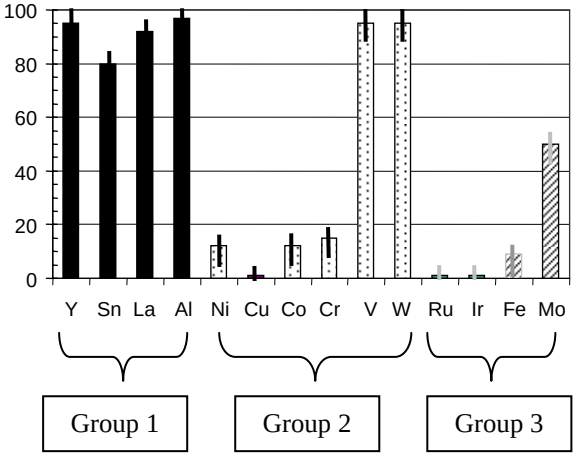

Table 1: Percentage of contamination remaining in oxide after the oxidation

Group 1, 2 and 3 can damage surface, interface and oxide integrity. This is evidenced by SE, AFM, Haze, I(V), C(V) and will be presented in the full extend of the paper.

Conclusion

Thanks to physical short loops (lifetime, thickness, contamination analysis) and to an as exhaustive as possible list of metallic elements candidate in advanced microelectronics, this paper estimates the seriousness of cross-contamination that the new devices might introduce into IC manufacturing lines.

References

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